REMARKS

Prior to entry of this paper, claims 1-16 and 18-24 were pending. Claim 23 was allowed. In this paper, Claims 21, 22, and 24 are amended, and Claims 11, 13-16, and 18-20 are cancelled. Claims 1-10, 12, and 21-24 are currently pending. No new matter is added by way of this amendment. For at least the following reasons, Applicants respectfully submit that each of the presently pending claims is in condition for allowance.

Allowed Subject Matter (Claim 23)

Applicants appreciate the indication that Claim 23 is allowed and thank the Examiner for his work on this matter.

Rejection to Claims 21-22 and 24 under 35 U.S.C. §112

Claims 21-22, and 24 were rejected under 35 U.S.C. §112, second paragraph as being indefinite.

First, Claims 21 was rejected as there being no antecedent basis for, "the first current" in claim 21 on line one of page 6. Applicant respectfully traverses this rejection. Antecedent basis for "the first current" appeared at the beginning of the Claim ("a current source that is operable to provide **a first current**" [emphasis added]).

Second, Claims 21 and 22 were rejected as VDD not being given an explicit definition. This rejection is respectfully rendered moot based on the amendment to Claims 21 and 22.

Third, Claim 24 was rejected as "the current" on lines 2-3 of page 7 lacking antecedent basis. This rejection is respectfully rendered moot based on the amendment to Claim 24.

Fourthly, Claim 24 was rejected as being misdescriptive to state a connection between elements being made through a ground connection (i.e. "and the source of the n-type transistor is coupled to the second node"). This rejection is respectfully traversed. It is respectfully submitted that there is nothing misdescriptive in Claim 24. A ground node is a valid node in a circuit to which elements may be coupled.

Rejection to Claims 1-16, 18-20, 22 and 24 under 35 U.S.C. §102

Claims 1-16, 18-20, 22, and 24 were rejected under 35 U.S.C. §102(b) as being anticipated by Kong et al. (U.S. Patent No. 6,242,973, hereinafter Kong).

The rejection to Claims 11, 13-16, and 18-20 are respectfully rendered moot in light of the cancellation of Claims 11, 13-16, and 18-20.

Claims 1-10

The rejections to Claims 1-10 are respectfully traversed.

Claim 1 is respectfully submitted to be allowable at least because Kong does not disclose, "at a voltage threshold of the logic circuit, a source-to-gate voltage of the p-type transistor is greater than a mid-supply voltage of the logic circuit, and the gate-to-source voltage of the n-type transistor is greater than the mid-supply voltage", as recited in Applicant's Claim 1.

The Office Action states, "It can be seen that the p-type's (M1), do to the bootstrapping ability of circuit 100, the source to gate voltage is higher than the mid-supply voltage. When there is a low signal input to it, the gate-to-source voltage is about VDD. VDD is twice that of the mid-supply voltage. Thus it is greater. This bootstrapping function also makes n-type transistor (M2) greater than its gate-to-source voltage."

Applicant respectfully disagrees. Claim 1 requires that at one particular point in time (the voltage threshold of the logic circuit), the source-to-gate voltage of the p-type transistor and the gate-to-source voltage of the n-type transistor both be greater than the mid-supply voltage. When a low signal is input to the gate of transistor M1 (which occurs when IN is high), the source-to-gate voltage will become greater than VDD, because the voltage at the gate of M1 will become less than VSS due to the capacitive coupling. The source-to-gate voltage of transistor M1 will become about 2*VDD. However, when this occurs, the voltage at the gate of transistor M2 is coupled to VSS, because transistor M8 is closed, so the gate-to-source voltage of transistor M2 is about zero. Accordingly, when the voltage input to the gate of transistor M1 is a low signal, the gate-to-source voltage of transistor M2 is less than the mid-supply voltage.

Claims 2-10 are respectfully submitted to be allowable at least because they depend on Claim 1, which is proposed to be allowable.

It is respectfully submitted that Claim 3 is also allowable at least because Kong does not disclose, "the voltage offset circuit includes a resistor circuit", as recited in Applicant's Claim 3.

The Office Action cited a definition of Ohm's law, which is a correct definition, and a definition which a capacitor does not meet. "The result is a current whose magnitude depends on the characteristics of the piece of material and the applied voltage." What is implicit, but not explicitly stated, is that, the current depends on the characteristics of the piece of material and the applied voltage, but does NOT depend on time. Ohm's law is I=V/R. However, current for a capacitor follows the equation I=C*dV/dt. Ohm's law states that the current is simply proportional to the voltage across the piece of material. In a capacitor, the current is proportional to the rate of change of the voltage. Therefore, it does not follow Ohm's law. In fact, a resistor, or a conductor that acts like a resistor is sometimes referred to as "ohmic", because it obeys Ohm's law. A capacitor is known to be "non-Ohmic", because it does not obey Ohm's law. See, for example, "Ohm's Law" at http://www.physics.uoguelph.ca/tutorials/ohm/Q.ohm.intro.html. It states:

"1. **Ohm's Law** deals with the relationship between voltage and current in an ideal conductor. This relationship states that:

The potential difference (voltage) across an ideal conductor is proportional to the current through it.

The constant of proportionality is called the "resistance", **R**.

Ohm's Law is given by:

V = I R

where V is the potential difference between two points which include a **resistance** R. I is the current flowing through the resistance. For biological work, it is often preferable to use the **conductance**, g = 1/R; In this form Ohm's Law is:

I = g V

2. Material that obeys Ohm's Law is called "**ohmic**" or "**linear**" because the potential difference across it varies linearly with the current."

Also, it is respectfully submitted that Claim 4 is also allowable at least because capacitors Cp and Cn are not "resistive elements."

Claim 12

The rejection to Claim 12 is respectfully traversed. It is respectfully submitted that Kong does not disclose, "the voltage offset circuit includes a resistor circuit", as recited in Applicant's Claim 12.

Claim 22

The rejection to Claim 22 is respectfully traversed. It is respectfully submitted that Kong does not disclose, "the voltage offset circuit is operable to provide the first and second voltages such that the logic circuit performs as if the difference between the high power supply and the low power supply was approximately 3*VDD/2". As recited in Applicant's Claim 22. The Office Action states that the value of VDD can be "defined as any voltage", and therefore, limitation is automatically met.

Applicant respectfully disagrees. The high power supply voltage VDD could be selected to have a variety of different voltages, depending on the application. However, the claim language requires that, whatever voltage is used for the power supply voltage VDD in the circuit, the logic circuit performs as of the difference between high power supply VDD and lower power supply VSS were 1.5 times greater than the actual difference between VDD and VSS. Thus, if VDD=1.5V and VSS=0V, the circuit performs as if VDD were 2.25V. However, if VDD=2.0V and VSS=0V, the circuit performs as if VDD were 3.0V. This is not arbitrary; the performance is based on the actual voltage difference between the power supplies used in the circuit.

Claim 24

The rejection to Claim 24 is respectfully traversed at least because Kong does not disclose, "regardless of the logic level at the gate of the p-type transistor, the capacitor circuit is coupled between the gate of the p-type transistor and the second node", as recited in Applicant's Claim 24. In Kong, capacitor Cp is de-coupled from the gate of transistor M1 when the input signal IN is low. When signal IN is low, transistor M4 operates like a switch that is turned off. A switch that is turned off performs a de-coupling function. It is true that an electrical switch, unlike a mechanical

switch, does not actually causing a physical separation between circuit elements; however, the result is the same, in an electrical switch such as a transistor performs essentially the same de-coupling function as a mechanical switch when the switch is off. When signal IN is low, capacitor Cp is cut off from the gate of transistor M1.

For at least these reasons, it is respectfully submitted that the rejections to Claims 1-10, 12, 22, and 24 under 35 U.S.C. §102 should be withdrawn.

Rejection to Claim 21 under 35 U.S.C. §103

Claim 21 was rejected under 35 U.S.C. §103(a) as being unpatentable by Kong in view of Sanwo et al. (U.S. Patent No. 6,472,906, hereinafter Sanwo). The rejection is respectfully traversed. Neither Kong nor Sanwo, singly or in combination, teach all of the claim limitations of Applicant's Claim 21.

First, neither Kong nor Sanwo, singly or in combination, teaches, "the voltage offset circuit is operable to provide the first and second voltages such that the logic circuit performs as if the difference between the high power supply and the low power supply was approximately VDD+I1*R1", as recited in Applicant's Claim 21. The Office Action states that the limitation is taught because VDD is an arbitrary value that could be anything. While it is true that different values for the high power supply voltage VDD could be used in difference applications, if a different value were used for the power supply voltage, VDD+I1*R1 would change accordingly. Therefore, it is not arbitrary.

Also, in the proposed combination, R2 would not be part of the voltage offset circuit. Applicant's Claim 21 recites, "a voltage offset circuit that is arranged to provide a first voltage to a gate of the p-type transistor, and further arranged to provide a second voltage to a gate of the n-type transistor such that the second voltage is positively offset relative to the first voltage, wherein the positive offset is less than the difference between the high power supply and the low power supply". If transistors M1 and M2 were replaced with open drain driver 60 of Sanwo, resistor R2 would not be part of the voltage offset circuit. The Office Action states, "R2 of Sanwo et al. the inverter INV was part of the voltage offset circuit." However, the voltage offset circuit of Claim 21 is defined as

a voltage offset of voltages provided to the inverter, not a voltage offset circuit that includes the inverter as part of it.

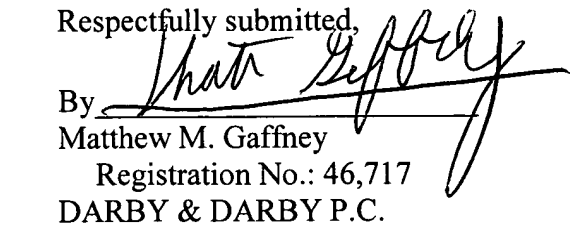
For at least these reasons, it is respectfully submitted that the rejection of Claim 21 under 35 U.S.C. § 103 should be withdrawn.

CONCLUSION

It is respectfully submitted that each of the presently pending claims (Claims 1-10, 12, and 21-24) are in condition for allowance and notification to that effect is requested. Examiner is invited to contact the Applicants' representative at the below-listed telephone number if it is believed that the prosecution of this application may be assisted thereby. Although only certain arguments regarding patentability are set forth herein, there may be other arguments and reasons why the claimed invention is patentable. Applicant reserves the right to raise these arguments in the future.

Dated: November 14, 2005

Respectfully submitted,

By 

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